

1/14

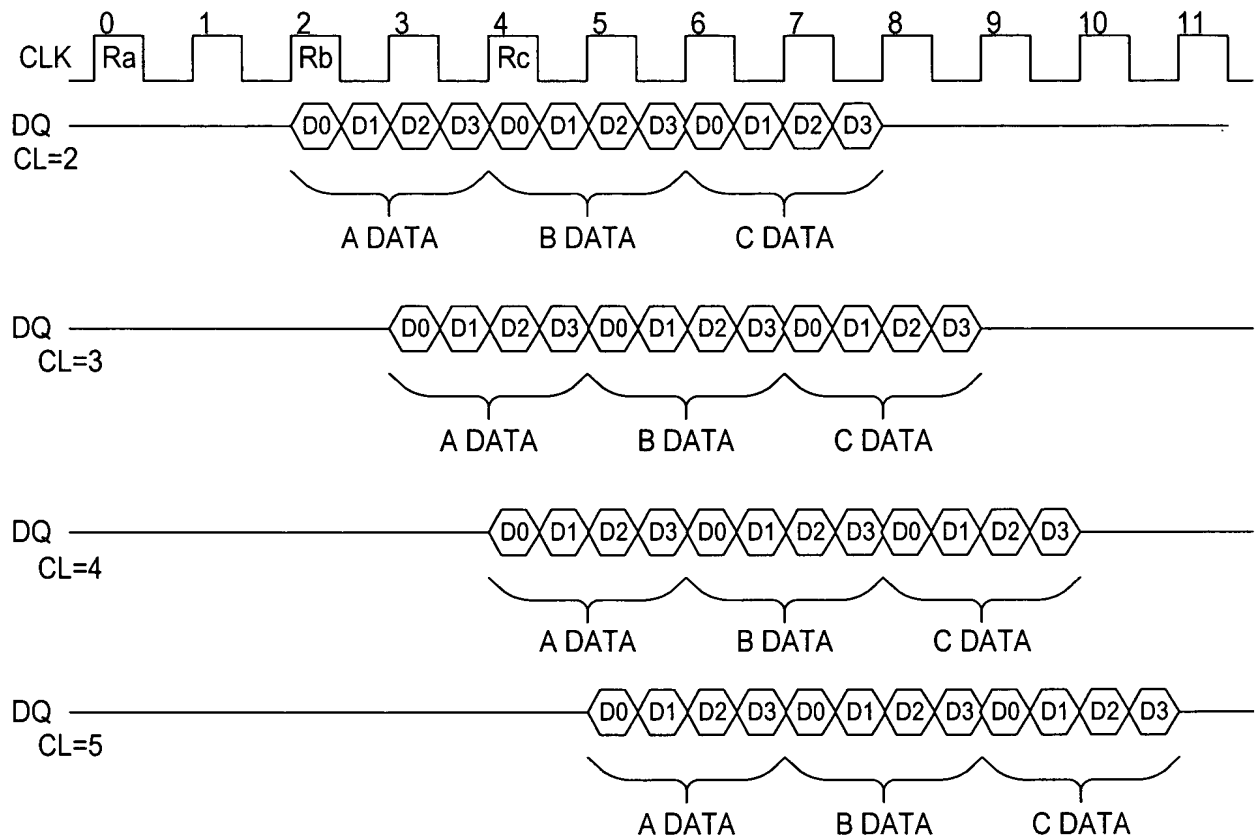


FIG. 1 PRIOR ART

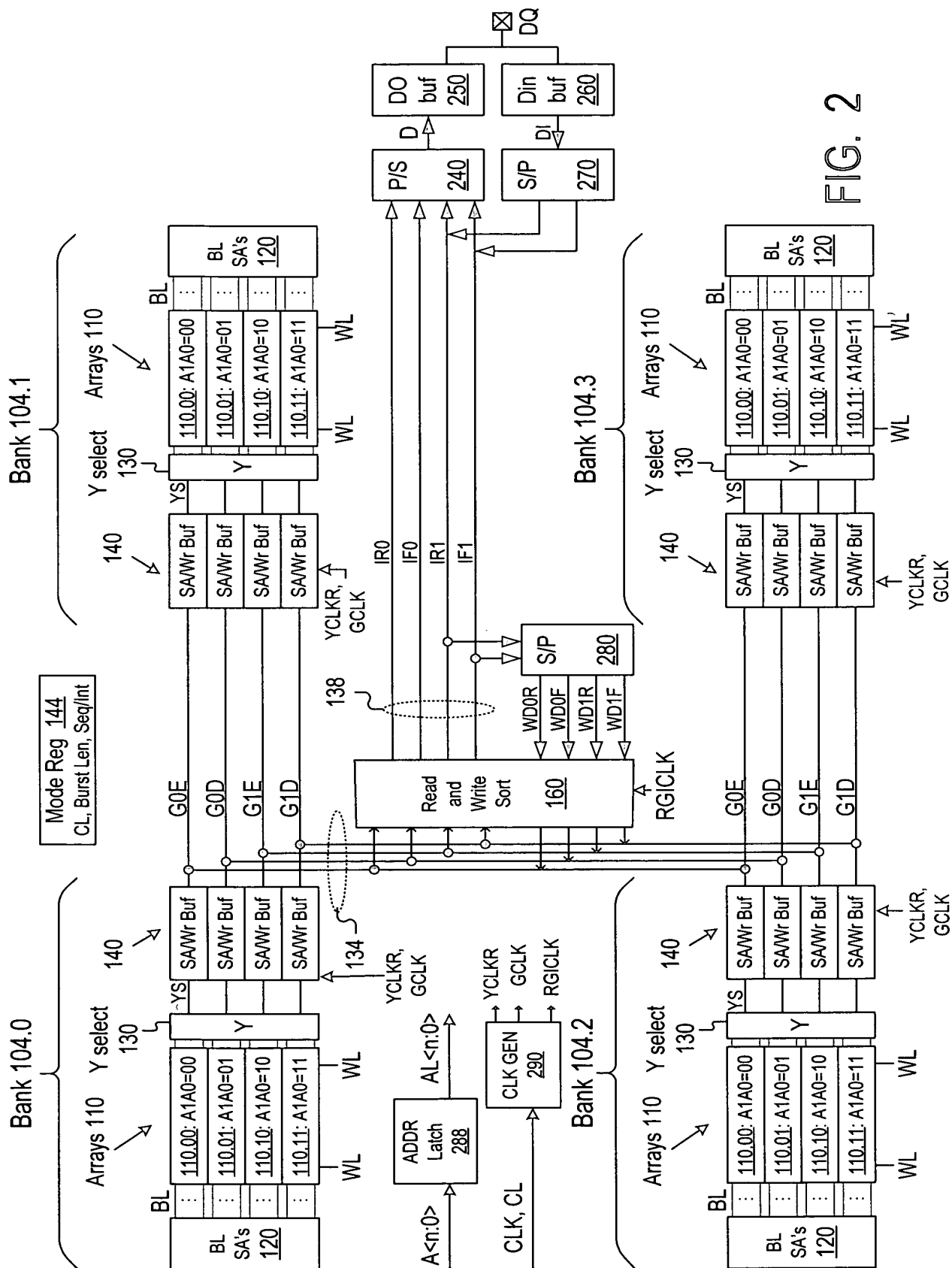
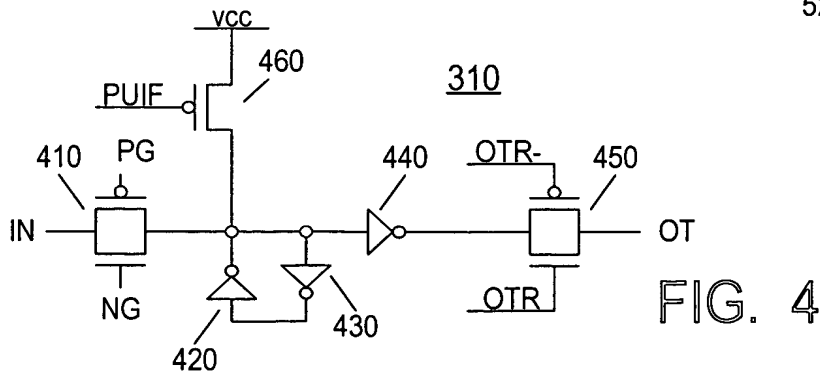
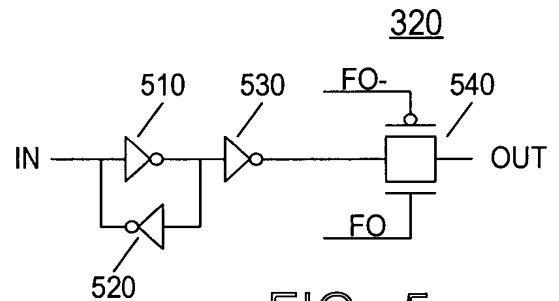
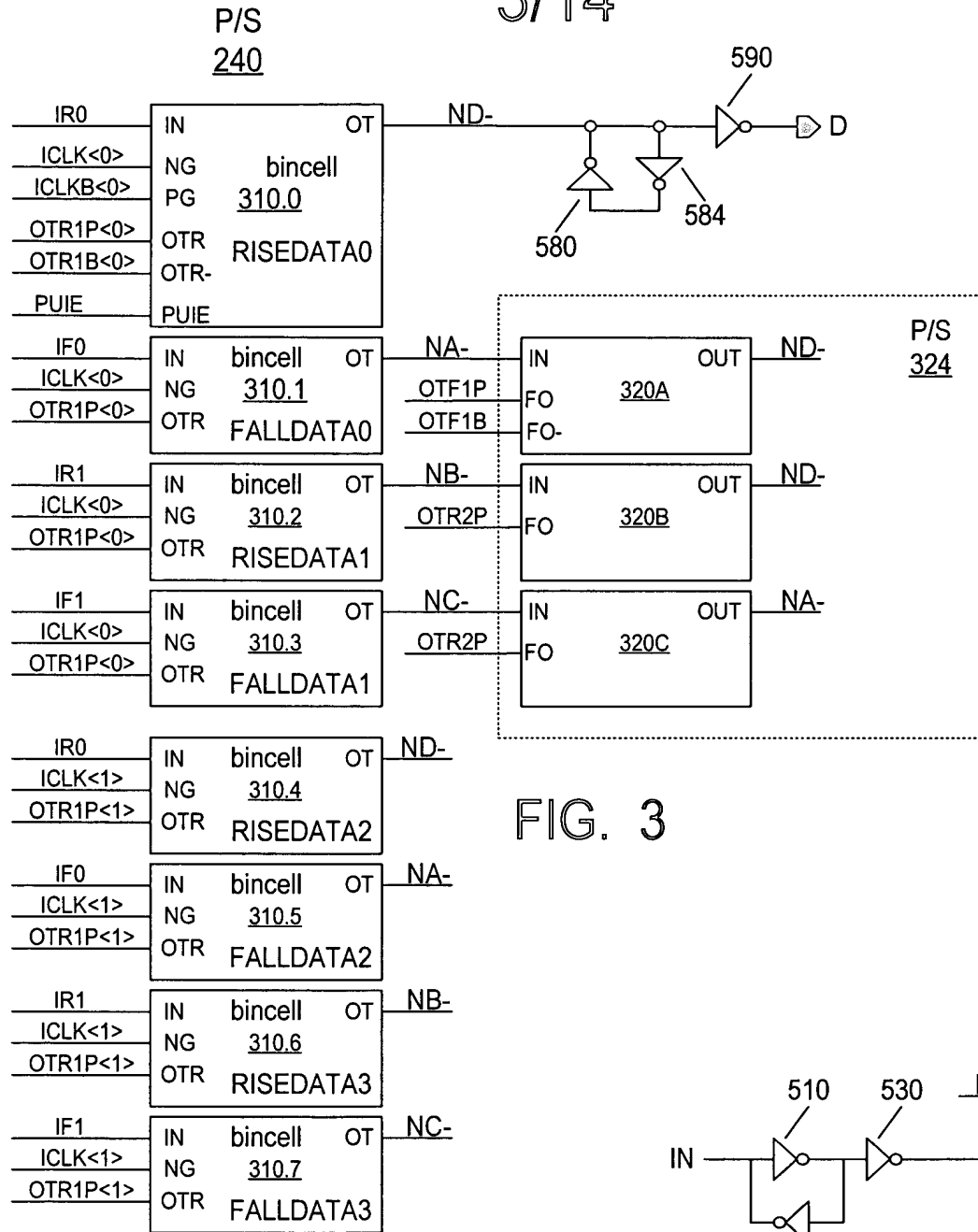


FIG. 2

3/14



4/14

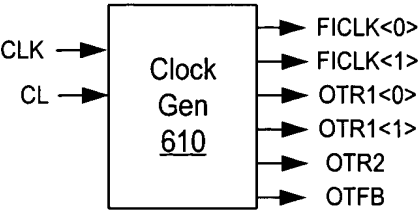


FIG. 6A

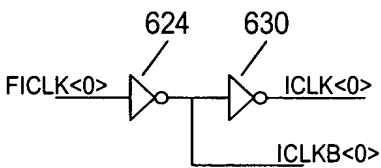


FIG. 6B

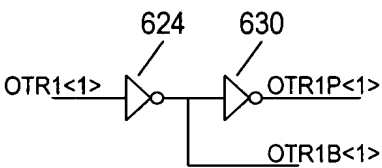


FIG. 6E

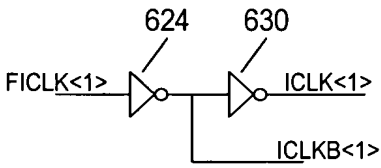


FIG. 6C

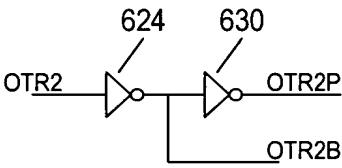


FIG. 6F

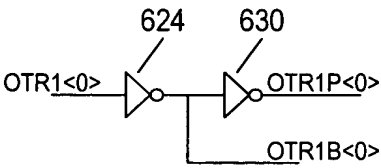


FIG. 6D

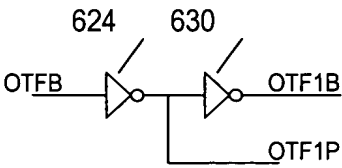


FIG. 6G

5/14

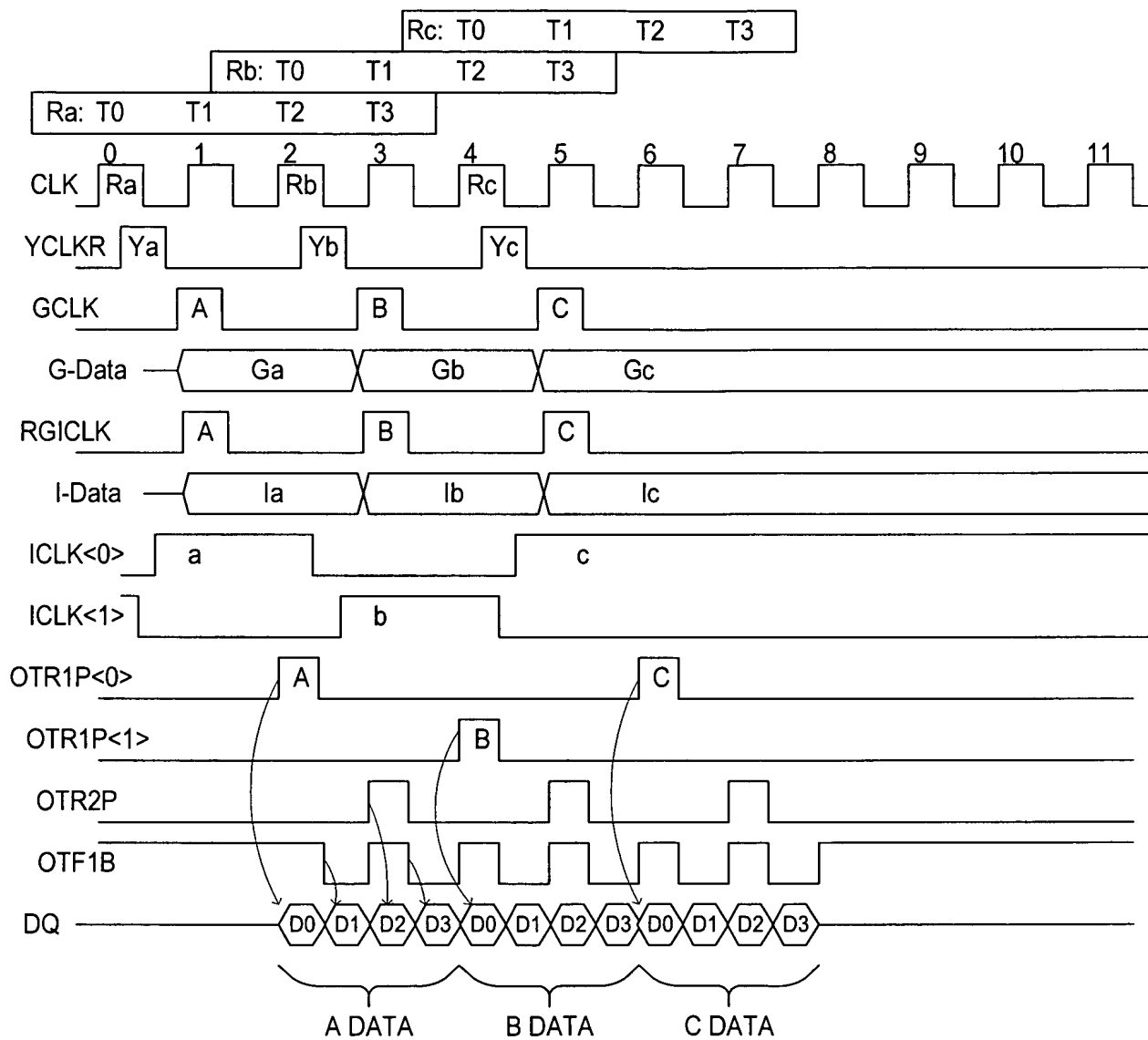
DDR2 CL=2 READ

FIG. 7

6/14

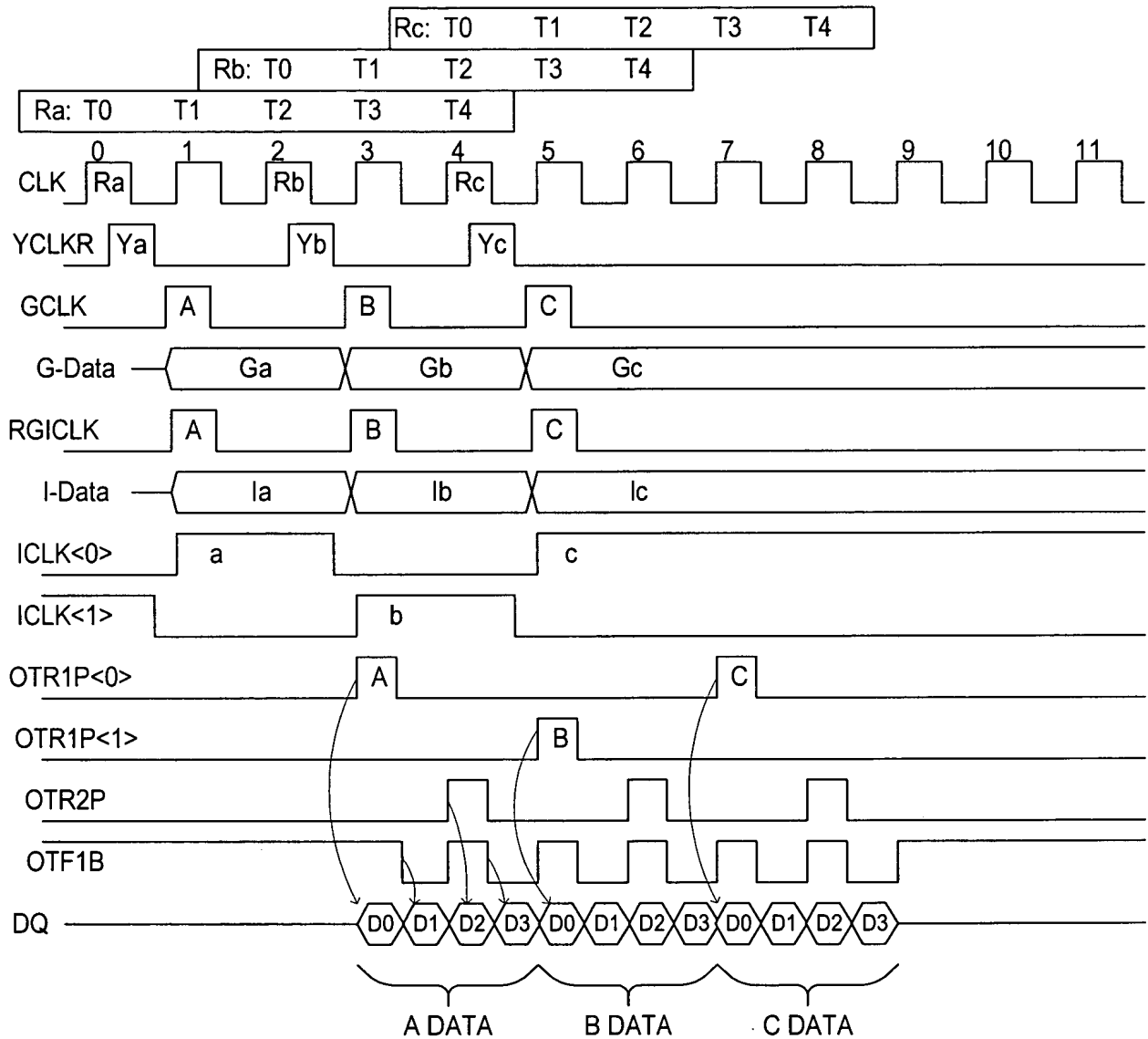
DDR2 CL=3 READ

FIG. 8

7/14

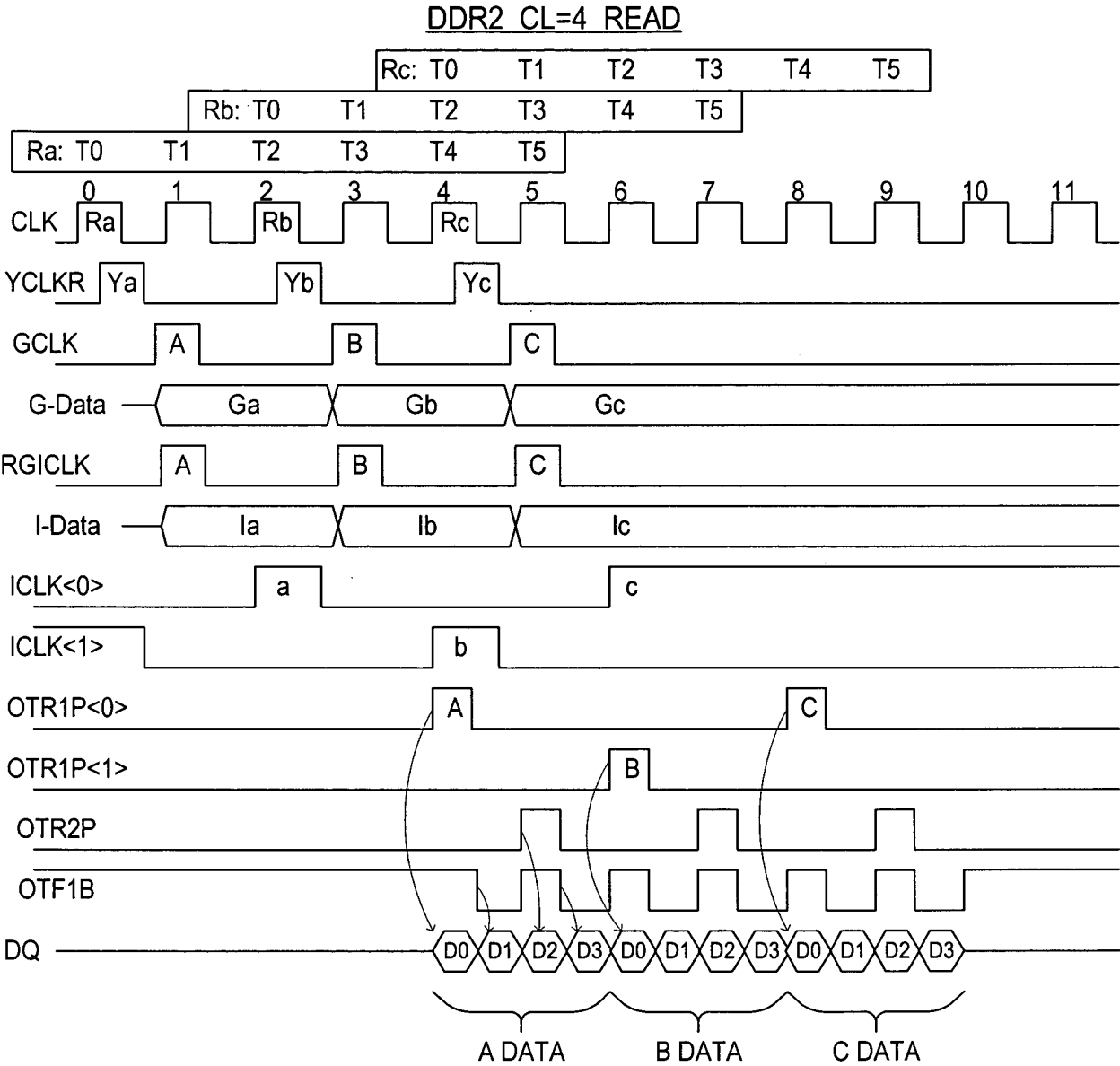


FIG. 9

8/14

DDR2 CL=5 READ

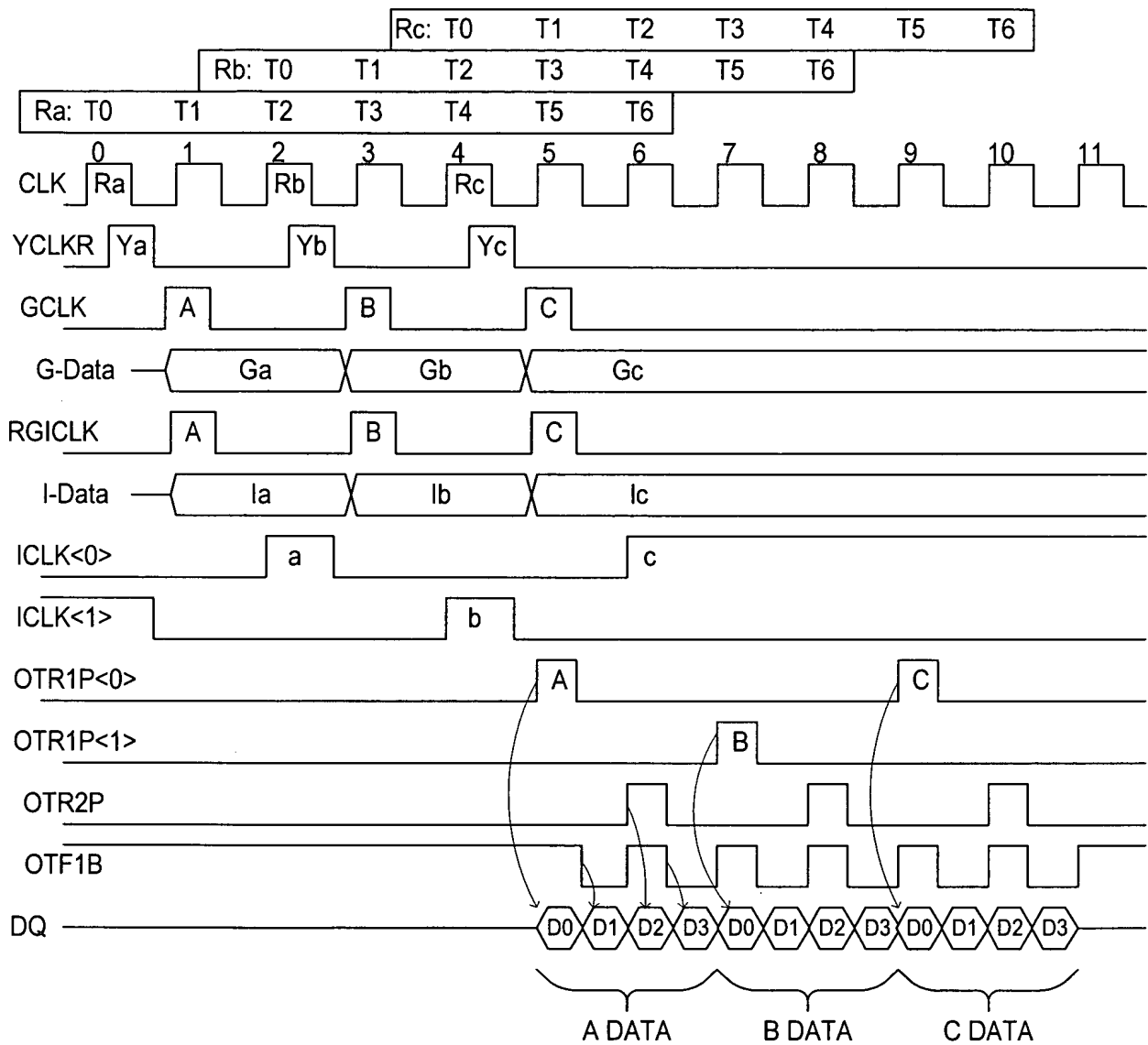


FIG. 10

9/14

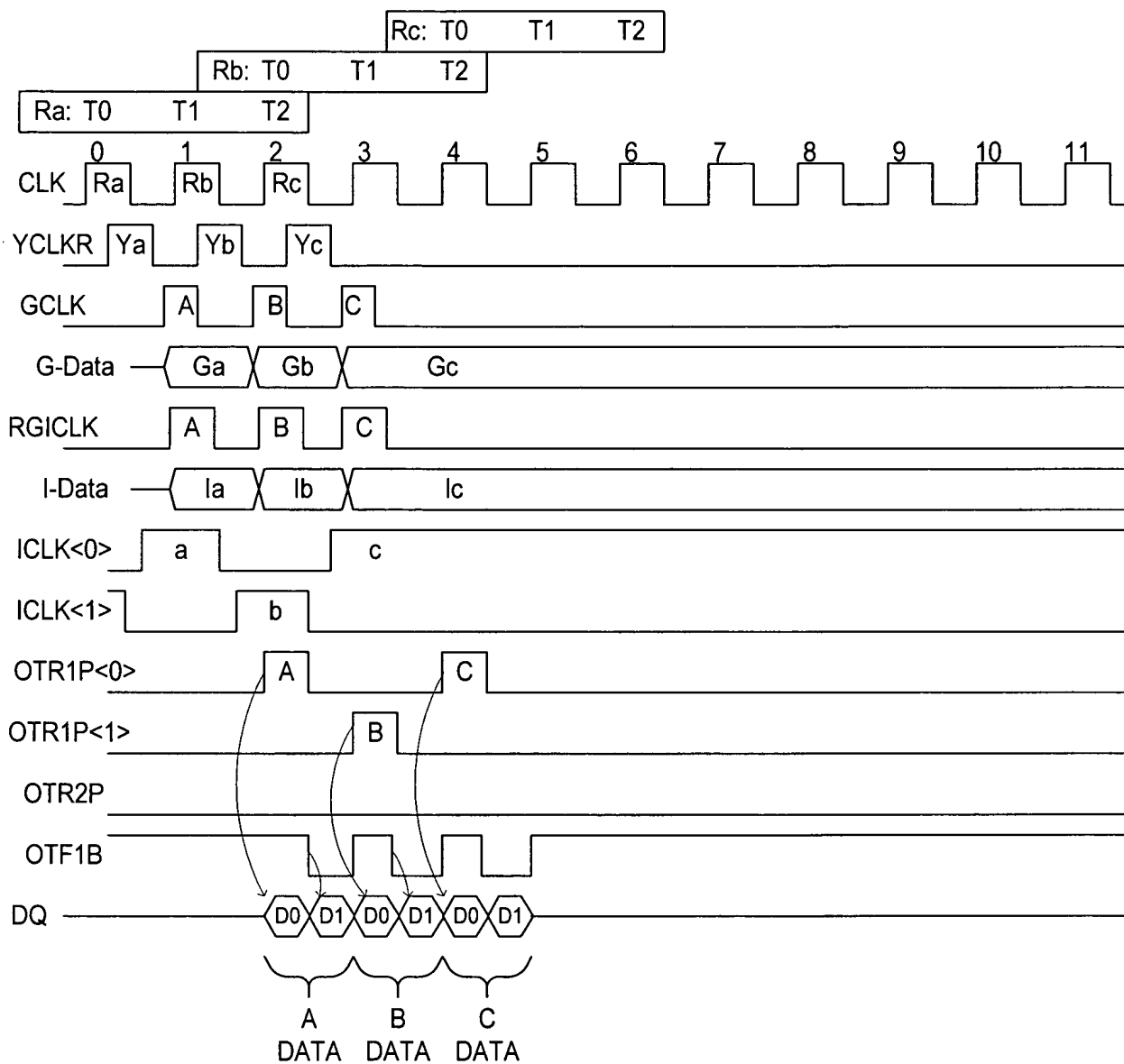
DDR1 CL=2 READ

FIG. 11

10/14

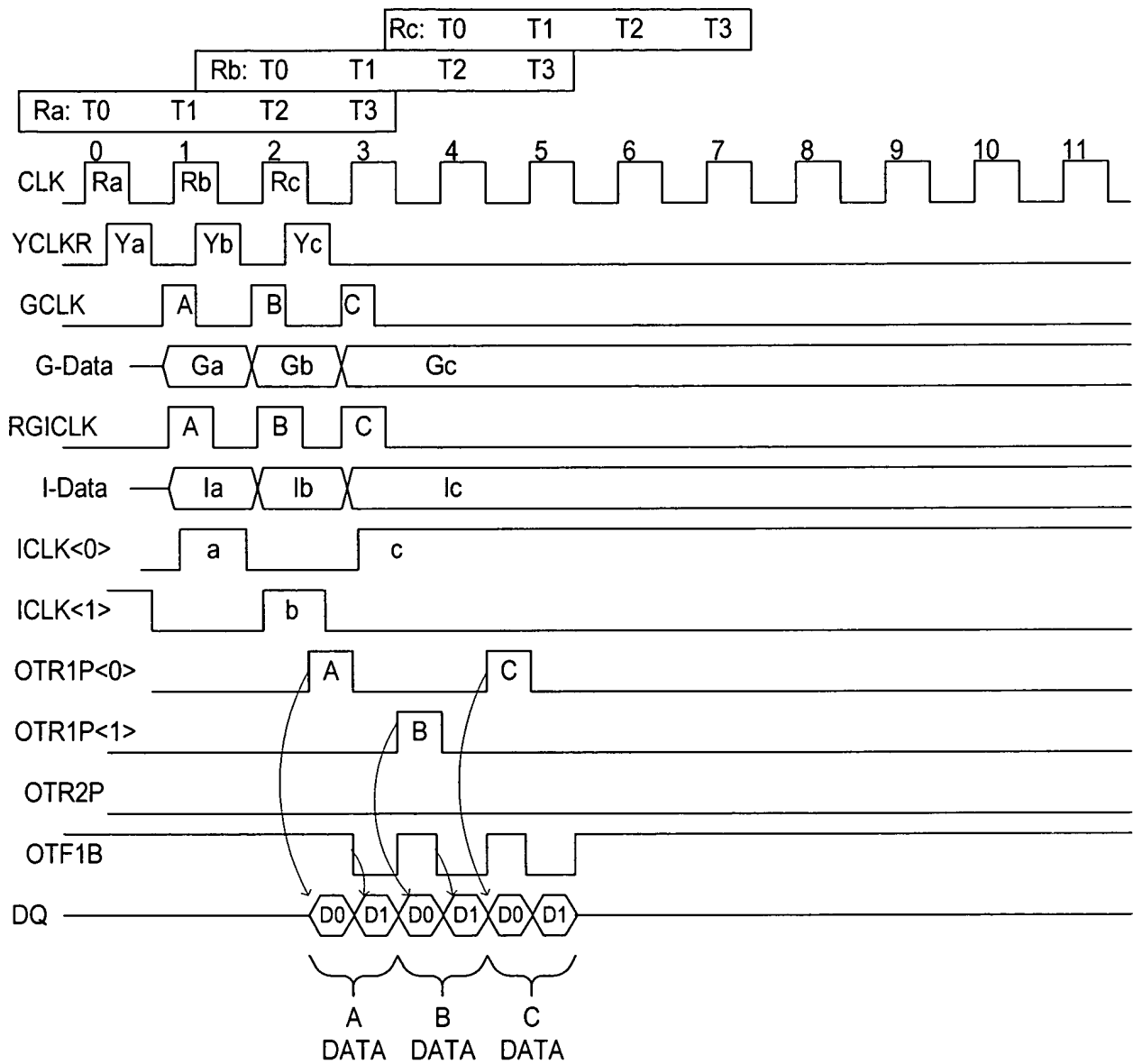
DDR1 CL=2.5 READ

FIG. 12

11/14

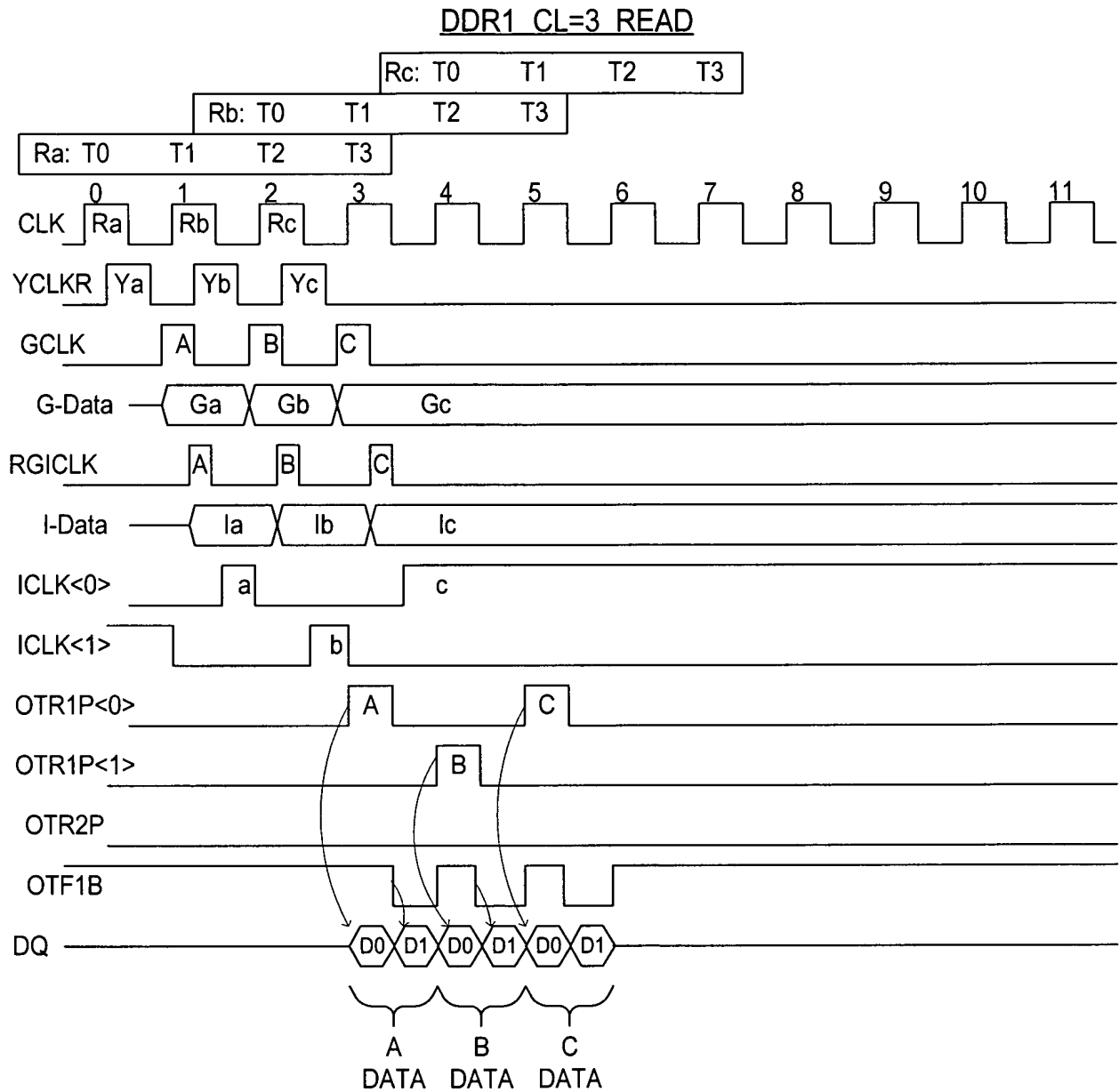


FIG. 13

12/14

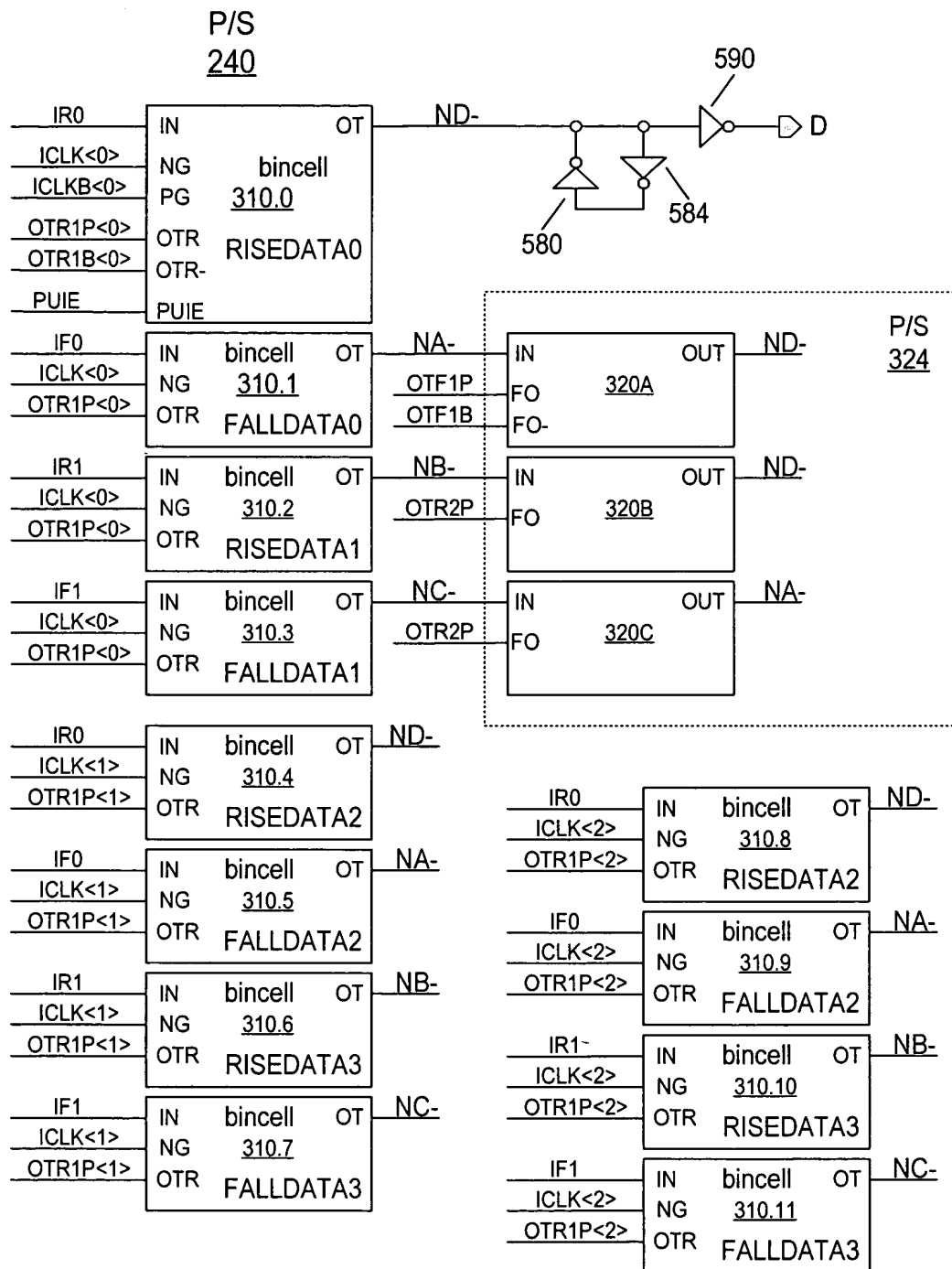
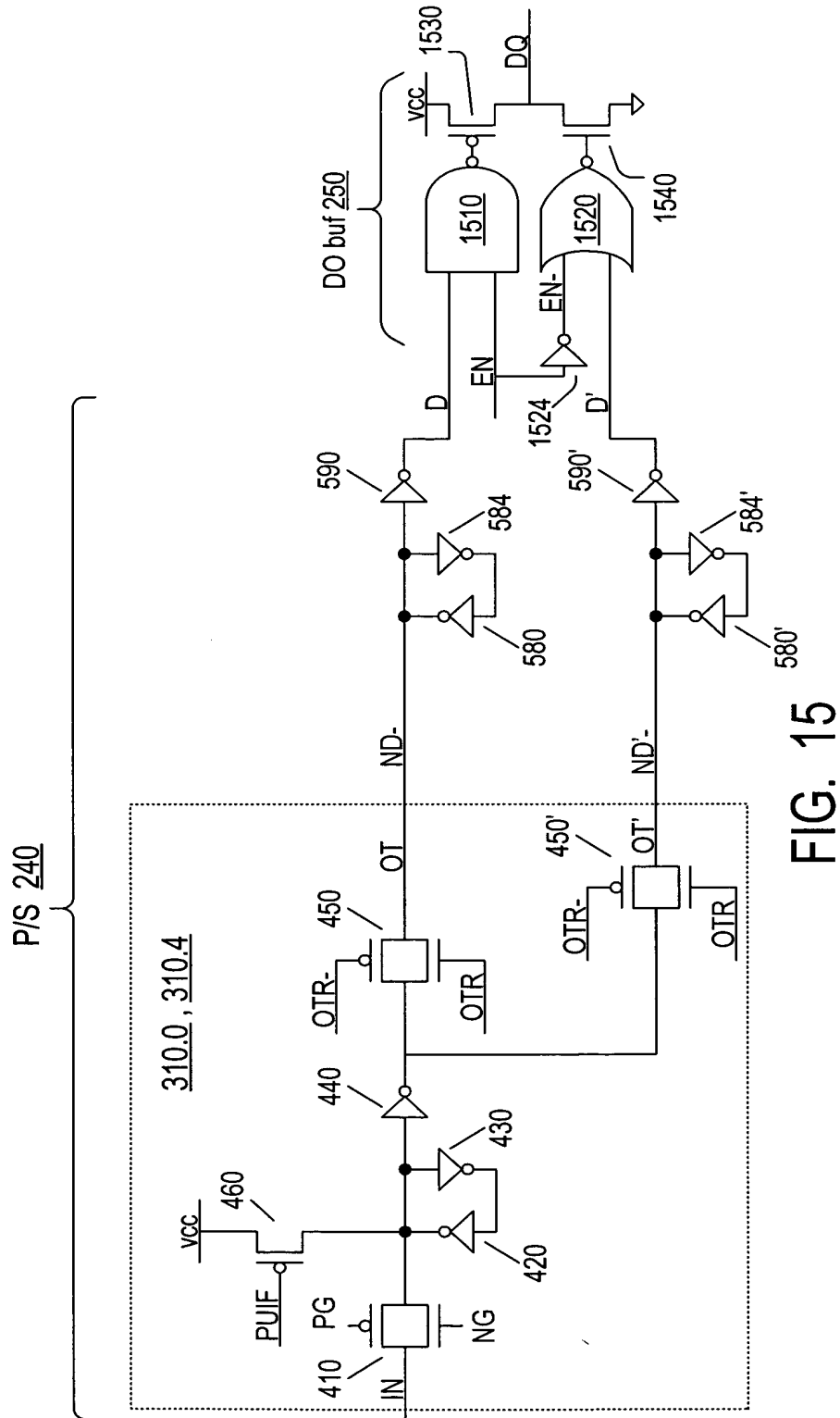


FIG. 14

13/14



14/14

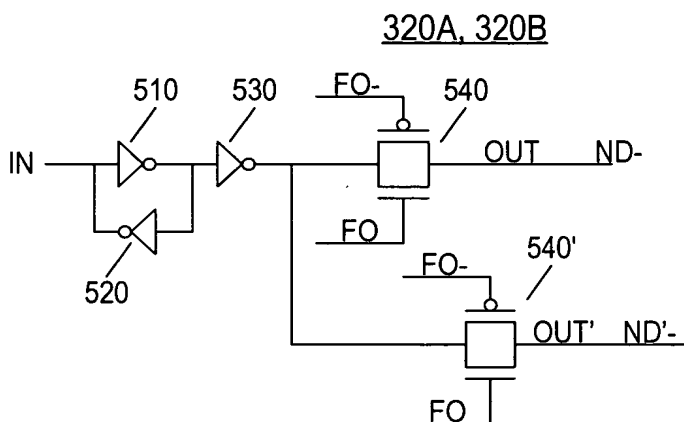


FIG. 16

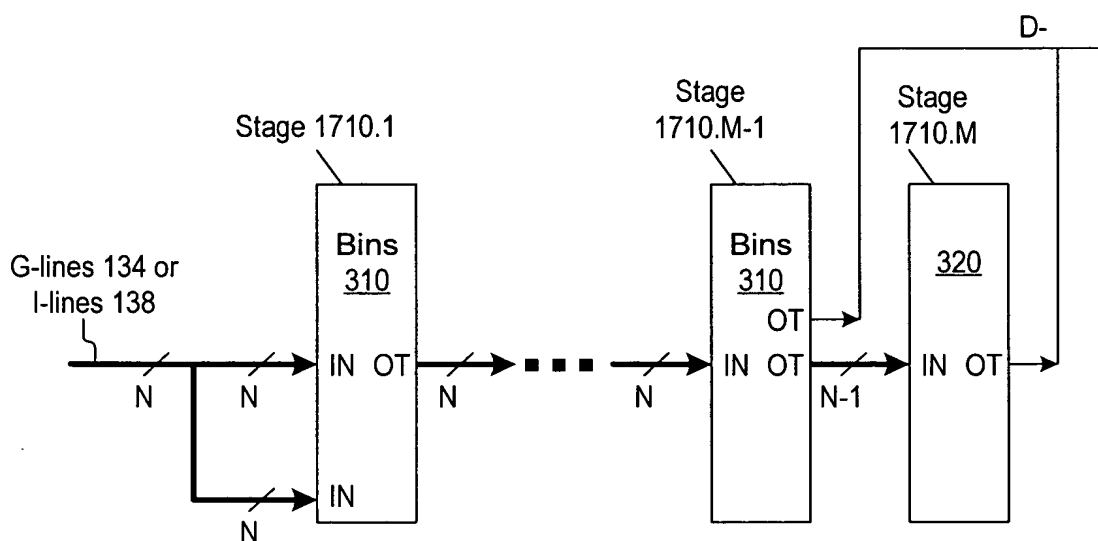


FIG. 17